Senior FPGA Engineer

Openings: 1 (Bangalore, India)

Experience: 5+

Job Description:

Looking for FPGA design engineer that can implement control logic state machines and DSP algorithms in FPGA fabric for high throughput medical devices. Requires excellent troubleshooting and debug skills for both simulation and in circuit.

Should have expertise in:

- Excellent knowledge of Digital Design.
- Excellent knowledge of clock-domain crossing.
- RTL Design in Verilog and System-Verilog.
- Creation of micro-architecture from High Level Specifications.
- Functional simulation with ModelSIM or similar tools
- FPGA Design and Synthesis.
- FPGA Map and Route flow, pin assignments, attribute assignments, resource fixing and design partitioning.
- Targeting designs for Intel(Altera) or Xilinx FPGAs.
- Xilinx Vivado or Intel Quartus Prime.
- IP creation and parametrization using Vivado or Quartus.
- Debug using ChipScope/SignalTap and Oscilloscopes/Protocol Analyzers.
- Knowledge of static timing analysis and timing closure using SDC.
- Working with cross-functional, global team of Hardware designers(PCB), Software Engineers(Firmware and App), Verification and Validation Engineers.
- Leading teams to successful completion of projects within deadlines.
- Excellent problem solving skills.

Good to have expertise in:

- Knowledge of TCL scripting and Python will be an added advantage
- Transceivers and PHY
- Power estimation and resource utilization estimation.
- Sot-processor cores like Microblaze or Nios-II
- Knowledge of Digital Signal Processing concepts will be an advantage.
- Knowledge of Matlab or Python for algorithm design will be an advantage.
- Knowledge of embedded systems/C/C++ will be an added advantage.

FPGA Engineer

Openings: 1 (Bangalore, India)

Experience: 3+

Job Description:

Looking for FPGA design engineer that can implement control logic state machines and DSP algorithms in FPGA fabric for high throughput medical devices. Requires excellent troubleshooting and debug skills for both simulation and in circuit.

Should have expertise in:

- Continual integration of unit modules into FPGA top level
- Extensive experience using SignalTap to debug logic and/or timing issues where software functional tests drive the FPGA data path logic
- Constructing bypass, data taps, and data pattern generators for isolation and unit/subsystem
- Timing closure, constraints file management, basic glue logic between DSP blocks
- Ability to do power estimation (Both pre implementation and post implementation)
- Working with board designer to give optimal pin out mappings
- Working with software team members to create, execute and debug unit level and system level verification tests
- HDL simulation tool: ModelSim or similar
- Verilog HDL/VHDL
- Xilinx/Altera FPGAs, Quartus II/Vivado/ISE and SignalTap/Chipscope
- Taking ownership of project and related tasks

Good to have expertise in:

- SoC and QSYS
- Protocols like AMBA, AXI, Avalon, USB, PCIe
- Memory interfaces like DDR2/DDR3/DDR4
- Control buses like I2C and SPI/QSPI